1.5 Gb/s, 6.6 mW 8-bit multiplexer using two-phase dynamic FET logic

Peter S. Lassen, Stephen I. Long[1]

Center for Broadband Telecommunications
Electromagnetics Institute, Build. 348
Technical University of Denmark
DK-2800 Lyngby, Denmark
[1] University of California, Santa Barbara, USA

Abstract

GaAs Two-Phase Dynamic FET Logic (TDFL) gates are used in the design of a high-speed, low-power 8-bit multiplexer. Operation of the multiplexer is demonstrated at 1.5 Gb/s with an associated power dissipation of 6.6 mW. The operation of the multiplexer demonstrates the high equivalent gate count of TDFL gates, direct compatibility between TDFL and Direct-Coupled FET Logic (DCFL), and the advantages of shift register architectures when simple, low-power dynamic latches are available in GaAs circuits.

Introduction

The increasing emphasis on portable operation of computers and communications systems has placed a priority on low power circuit implementations. TDFL has been demonstrated to meet the requirements of very low power and high frequency performance concurrently with low voltage operation (V_{dd} from 1 to 1.5 volt) using a standard GaAs digital IC foundry process and dynamic logic circuit design techniques [1, 2].

TDFL gates are capable of performing all the standard logic functions (NOT, NAND, NOR, XNOR, AOI, etc.). They are non-ratioed, and have compact layouts. Furthermore, TDFL gates are compatible with static DCFL and super-buffer FET logic (SBFL) gates. Because of its very low power dissipation and the compactness of its layout, TDFL is a candidate for GaAs VLSI.

TDFL principles of operation

The operation of TDFL gates can be understood with the aid of Fig. 1 which shows the schematic of two TDFL inverters in series and a timing diagram.

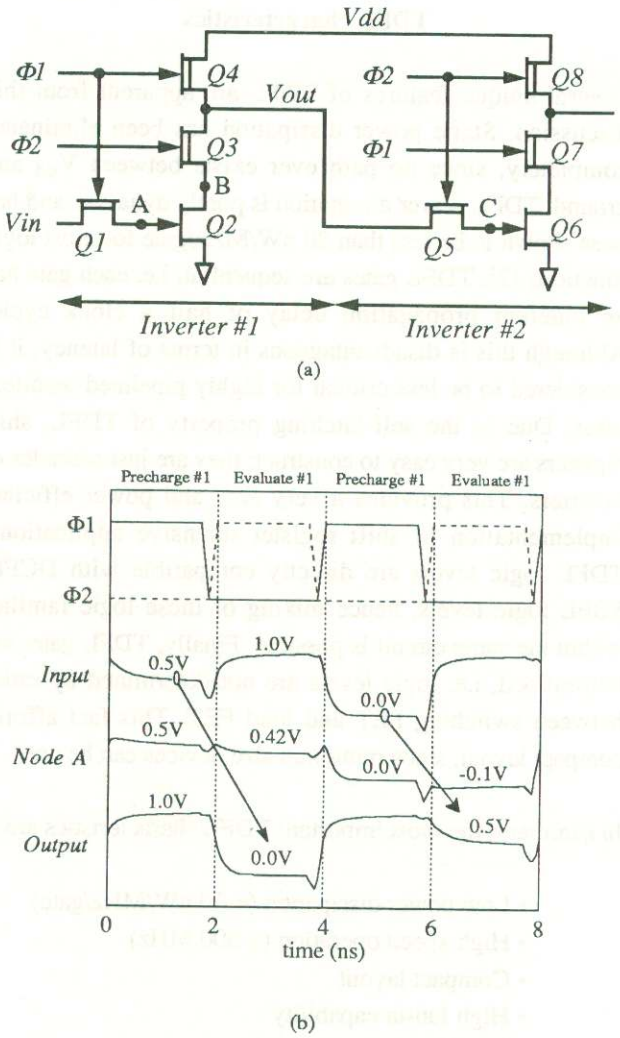

Fig. 1. (a) Schematic of two TDFL inverters in series.
(b) Simulated operation of inverter (V_{dd} = 1V).

TDFL gates operate from a single power supply (1V or greater) and two non-overlapping clock signals. When *Φ1* is high (precharge phase of operation of inverter #1), transistors *Q1* and *Q4* conduct, while *Q3* is cut-off. The output (*Vout*) is precharged to 1V, while node A is charged to +0.5V if the input (*Vin*) is high, or discharged to 0V if the input is low. After *Φ1* has gone low, *Φ2* goes high

(evaluate phase of inverter #1), and *Q3* and *Q5* conduct. If node A had been charged high during the precharge phase of operation, then the E-mode FET *Q2* conducts, and the output is discharged to ground through *Q2* and *Q3*. Had node A been discharged during the precharge phase, then *Q2* remains off, the output remains high, and a logic high level is passed to the input of inverter #2. Note, that the high level settles at about +0.5V, which is due primarily to gate-to-source conduction of *Q6*, though charge sharing between the output node and nodes B and C is partly responsible as well.

TDFL characteristics

Several unique features of TDFL are apparent from this discussion. Static power dissipation has been eliminated completely, since no path ever exists between V_{dd} and ground. TDFL power dissipation is purely dynamic, and has been shown to be less than 20 nW/MHz/gate for most logic functions [2]. TDFL gates are sequential, i.e. each gate has an inherent propagation delay of half a clock cycle. Although this is disadvantageous in terms of latency, it is considered to be less critical for highly pipelined architectures. Due to the self-latching property of TDFL, shift registers are very easy to construct; they are just cascades of inverters. This provides a very area and power efficient implementation of shift register intensive applications. TDFL logic levels are directly compatible with DCFL/SBFL logic levels, hence mixing of these logic families within the same circuit is possible. Finally, TDFL gates are non-ratioed, i.e. logic levels are not determined by ratios between switching FET and load FET. This fact affords compact layout, since minimum size devices can be used.

In summary, the most important TDFL characteristics are

- Low power dissipation (< 20 nW/MHz/gate)
- High-speed operation (> 500 MHz)
- Compact layout
- High fan-in capability
- Provides all logic functions
- Self-latching
- DCFL/SBFL compatible

Adding up these characteristics, TDFL is a promising candidate for GaAs VLSI. TDFL is particularly well suited for pipelined architectures and shift register intensive applications such as digital signal processing applications and within communications systems.

Circuit design

A. Multiplexer

The 8-bit multiplexer is based on a shift register architecture applying two 4-bit shift register with parallel read (Fig. 2). The shift register is composed of four cascaded sections each containing a 2,1 And-Or-Invert (21AOI) gate and an inverter. Each section is equivalent to a DFF with a selector on the input. Every fourth clock cycle, a sampling pulse (*read*) loads the four parallel data signals (*d1-d4*) into the shift register. The data are serialised by shifting it out during the next three clock cycles.

By taking advantage of the TDFL/DCFL compatibility, the output bit stream of two such 4-bit shift registers can be interleaved in a static DCFL AND gate, to produce an output bit rate at twice the clock frequency (Fig. 3). By inserting a TDFL inverter between one of the shift registers and the static AND gate, the data signals at nodes A and B will be shifted half a clock cycle relative to each other, due to the sequential two-phase operation of TDFL gates. The data values at nodes A and B are alternatingly merged in the static AND gate, since the output of a TDFL gate is charged high during the precharge phase of operation.

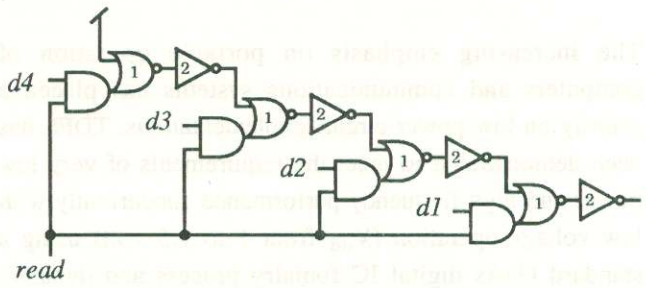

Fig. 2. 4-bit shift register with parallel read

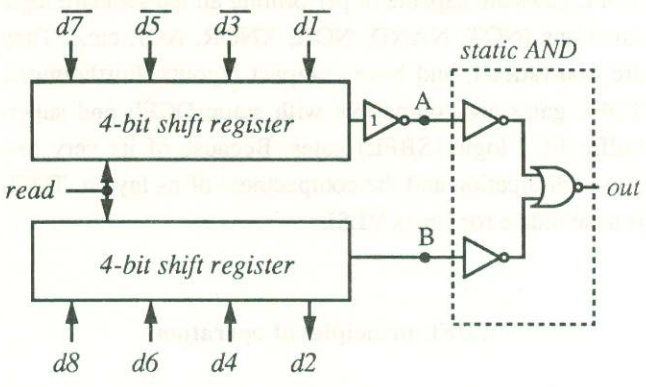

Fig. 3. 8-bit multiplexer

The total gate count of the multiplexer core is only 17 TDFL gates and 3 DCFL gates, demonstrating the high equivalent gate count of the TDFL multiplexer. A fully static implementation using DCFL requires approximately 100 DCFL NOR gates.

B. Control

The control circuit used for generating the *read* pulse for the multiplexer is based on a 4-bit shift register ring with preload (Fig. 4). The shift register is preloaded with a single logic '0' and three '1's when *init* is high. When *init* goes low, the logic '0' will propagate through the ring with a cycle time of four clock cycles, hence producing a *read* pulse every fourth clock cycle. The output section of the control circuit consists of a pass transistor (Φ2) and two SBFL buffers. The pass transistor 'filters out' the precharge phase from the *read* signal, while the buffers improve the drive capability.

C. Prescaler

For interfacing purposes, a 'byte clock' signal is generated on chip. This signal is used for synchronising the eight data input to external sources. The prescaler generates a 50% duty-cycle signal with a frequency of one fourth the clock frequency (i.e. input bit rate). The falling edge of the 'byte clock' signal is coincident with the read pulse, thus indicating when data is being loaded into the multiplexer shift registers.

The prescaler resembles a Johnson counter architecture, and consists of four TDFL gates connected in series with a static SBFL inverter in the feedback path (Fig. 5).

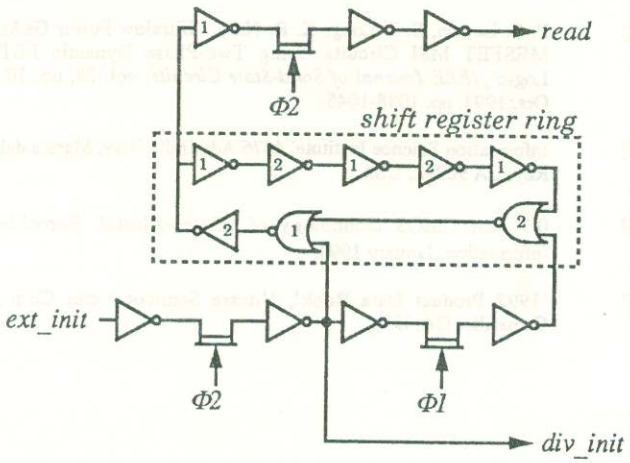

Fig. 4. Control circuit

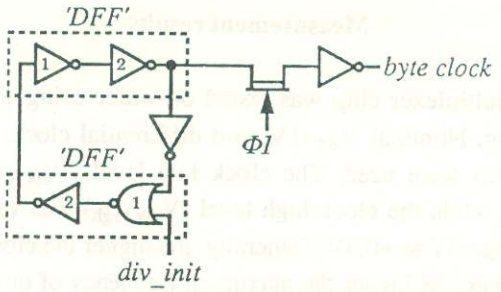

Fig. 5. Divide-by-four prescaler

The operation of the prescaler is most easily understood by considering two TDFL gates in series as an equivalent DFF. When *div_init* is high, the outputs of the two 'DFF's are constant high, and when *div_init* goes low, the two '1's will propagate through the ring, being inverted once every round trip. The bit pattern at the byte clock output will therefore be 11001100... with a frequency of one fourth the clock signal.

Implementation

The circuit was fabricated in the Vitesse Semiconductor 0.8 µm E/D MESFET process (H-GaAsII) through the MOSIS/ISI foundry service [3]. A plot of the layout is shown in fig. 6. The total area occupied by the multiplexer, control and prescaler circuitry is less than 300x300 µm^2. This demonstrates the potential area savings when using TDFL, which is mainly attributed to the high equivalent gate count and compact layout of TDFL gates.

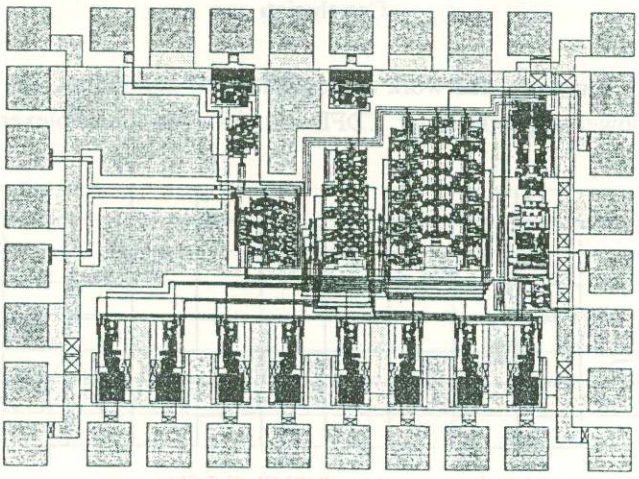

Fig. 6. Plot of multiplexer chip layout

Measurement results

The multiplexer chip was tested on-wafer using Cascade probing. Nominal V_{dd}=1V, and differential clock signals ($\Phi1/\Phi2$) were used. The clock low level ($V_{clk,low}$) was -1.2V, while the clock high level ($V_{clk,high}$) was varied in the range 0V to +0.3V. Generally, the higher the clock high level was, the higher the maximum frequency of operation. Fig. 7 shows multiplexer operation at 750 MHz, corresponding to an output bit rate of 1.5 Gb/s with $V_{clk,high}$=+0.3V.

In order to estimate the power dissipation of TDFL gates, power was measured as function of frequency at three different clock levels (Fig. 8). The slope of these curves represent the power dissipation of the TDFL gates, while the dc intercept represents the static power dissipated by the DCFL/SBFL gates. All measurements show a linear dependence on frequency. The average slope is 0.7 µW/MHz, which correpsonds to less than 14 nW/MHz/TDFL gate. The average dc intercept is 6.1 mW (135 µW/static gate). For comparison, a representative 0.7µm, 3.3V CMOS gate dissipates in the order of 3µW/MHz/gate [4]. However, because CMOS is a static logic approach, not every gate will be switching in every clock cycle as is the case with TDFL, and the duty factor will vary greatly with the application (a range of 0.1 to 0.4 may be typical). Even taking the duty factor into account, TDFL gates still dissipates in the order of 10 times less power than CMOS.

The total power dissipation of the 8-bit multiplexer chip is less than 150 mW including power dissipation of ECL I/O buffers. This compares favourably with 8-bit multiplexers implemented using static logic families in the same technology (e.g. 1.25 Gb/s @ 1.9 W, VS8011 [5]].

Conclusion

In summary, this work demonstrates the high-speed, low power capabilities of TDFL circuits. 8-bit multiplexer

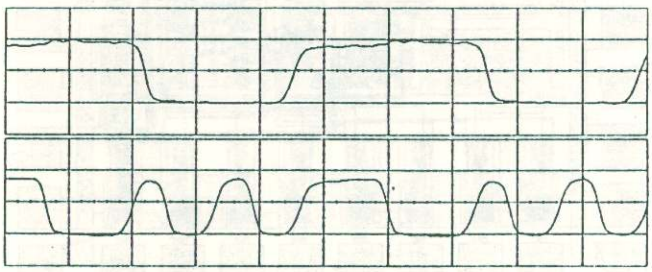

Fig. 7. Multiplexer operation at 750 MHz (1.5 Gb/s).
Top trace: byte clock signal, bottom trace: mux output.
Vert.: 500 mV/div, Hor.: 1 ns/div.

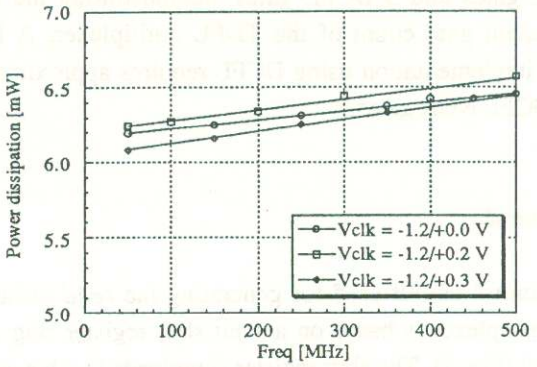

Fig. 8. Speed vs. Power (V_{dd}=1V)

operation was demonstrated at 1.5 Gb/s with an associated V_{dd} power dissipation of 6.6mW. This circuit demonstrates mixing of TDFL with low power static logic gates (DCFL/SBFL), high equivalent gate count and compact layout of TDFL circuits. These characteristics make TDFL an attractive candidate for GaAs VLSI. In particular, TDFL is suited for pipelined and shift register intensive applications.

Acknowledgements

The authors would like to acknowledge Dr. Kevin R. Nary at Rockwell International Science Center, CA., for helpful discussions, and Prof. S. Butner of the University of California, Santa Barbara, for CAD support.

References

[1] K. R. Nary, S. I. Long, 'GaAs Two-Phase Dynamic FET Logic : A Low-Power Logic Family for VLSI', *IEEE Journal of Solid-State Circuits*, vol. 27, no. 10, Oct. 1992, pp. 1364-1371.

[2] P. S. Lassen, S. I. Long, K. R. Nary, 'Ultralow-Power GaAs MESFET MSI Circuits Using Two-Phase Dynamic FET Logic', *IEEE Journal of Solid-State Circuits*, vol. 28, no. 10, Oct. 1993, pp. 1038-1045.

[3] Information Science Institute, 4676 Admiralty Way, Marina del Rey, CA 90292, USA.

[4] 0.7 µm CMOS technology of Mietec-Alcatel, Eurochip Information, January 1994.

[5] '1992 Product Data Book', Vitesse Semiconductor Corp., Camarillo, CA, USA.